ABSTRACT

A multi-selection prescaler for dividing an input signal according to a ratio to obtain a desired frequency. The circuit has of a plurality of logic gates and D-flip-flops: a first frequency divider for receiving an input signal and generating a divided frequency; a second frequency divider connected to the first frequency divider for performing a further frequency division based on a selection switch having a plurality of selection signals and a plurality of AND gates; a module control for performing a logic operation on the selection signals and an external control signal (MC) by OR gates and being connected to the first frequency divider to control the divided frequency of the first frequency divider; and an output selection circuit connected to the second frequency divider for selecting output signal according to the selection signals.